IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of: **Akio Itoh** Group Art Unit: **2815**

Serial No.: **09/594,091** Examiner: **Matthew E. WARREN**

Filed: **June 15, 2000** Confirmation No.: **8583**

For: **SEMICONDUCTOR MEMORY DEVICE HAVING PLANARIZED UPPER SURFACE AND A SION MOISTURE BARRIER**

Attorney Docket Number: **000761**
Customer Number: **38834**

SUBMISSION OF APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

December 2, 2004

Sir:

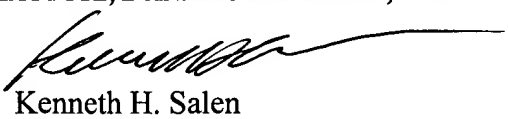
Submitted herewith is an Appeal Brief in the above-identified U.S. patent application.

Attached please find a check in the amount of $340.00 for the Appeal Brief fee.

If any additional fees are due in connection with this submission, please charge Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



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APPEAL BRIEF FOR APPELLANT

Ex parte Akio ITOH

SEMICONDUCTOR MEMORY DEVICE HAVING PLANARIZED UPPER SURFACE AND A SION MOISTURE BARRIER

Serial Number: 09/594,091

Filed: June 15, 2000

Examiner: Matthew Warren

Group Art Unit: 2815

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Date: **December 2, 2004**

(I) REAL PARTY IN INTEREST

The real party in interest is Fujitsu, Limited, by an assignment recorded in the U.S. Patent and Trademark Office on April 26, 2000, at Reel 010883, Frame 0671.

(II) RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to appellant, appellant's legal representative, or assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(III) STATUS OF CLAIMS

Independent claim 1 and dependent claims 2-4 are pending and rejected, and are appealed.

(IV) STATUS OF AMENDMENTS

This Appeal is filed following submission of an amendment by Appellant on March 10, 2004. An amendment dated March 10, 2004 was entered but finally rejected on June 2, 2004. No amendments were submitted by Appellant subsequent to the Final Rejection.

(V) SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 and dependent claims 2-4 are grouped and represented by the independently claimed subject matter of claim 1, which is characterized by the following limitations, which are supported in the specification in at least the following non-exclusive locations:

Claim	Specification Locations
1. (Previously Presented) A semiconductor device, comprising:	
a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed over the semiconductor substrate;	Page 10, line 10-19
a first insulating film formed over the transistor;	Page 9, line 22
a capacitor formed over the first insulating film, the capacitor having a dielectric film made of one of a ferroelectric material and a high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;	Page 16, line 7-12
silicon oxide film formed over the capacitor to form a planarized surface; wherein nitrogen resides all over the planarized surface of the silicon oxide film; and	Page 17, line 1-7
a wiring formed over the silicon oxide including nitrogen.	Page 11, line 14-19

Independent claim 5 and dependent claims 6-11 are grouped and represented by the independently claimed subject matter of claim 5, which is characterized by the following limitations, which are supported in the specification in at least the following non-exclusive locations:

Claim	Specification Locations
5. (Previously Presented) A semiconductor device, comprising:	
a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed over the semiconductor substrate;	Page 10, line 10-19
a first insulating film formed over the transistor;	Page 9, line 22
a capacitor formed over the first insulating film, the capacitor having a dielectric made of one of ferroelectric material and a high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;	Page 16, line 7-12
a second insulating film formed over the capacitor;	Page 17, line 1-7
a local interconnection formed over the second insulating film to electrically connect the upper electrode of the capacitor with the first impurity region;	Page 18, line 4-16
a third insulating film formed over the local interconnection and the second insulating film;	Page 18, line 19-27
a first wiring formed over the third insulating film and electrically connected to the second impurity region via a hole which is formed over the first insulating film, the second insulating film, and the third insulating film;	Page 19, line 1 to page 20, line 1
a fourth insulating film formed over the first wiring to serve an upper planarized surface, wherein nitrogen resides all over the upper planarized surface of the fourth insulating film; and	Page 20, line 2-7
a second wiring formed over the fourth insulating film including nitrogen.	Page 27, line 24 to page 29, line 7

Independent claim 12 is characterized by the following limitations, which are supported in the specification in at least the following non-exclusive locations:

Claim	Specification Locations
12. (Previously Presented) A semiconductor device, comprising:	
a transistor having a first impurity region and a second impurity region formed over a semiconductor substrate, and a gate electrode formed over the semiconductor substrate;	Page 10, line 10-19
a first insulating film formed over the transistor;	Page 9, line 22
a capacitor formed over the first insulating film, the capacitor having a dielectric film made of one of a ferroelectric material and a high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween; and	Page 16, line 7-12
a second insulating film formed over the capacitor to serve as an upper planarized surface; wherein nitrogen resides all over the upper planarized surface of the second insulating film; and	Page 12, line 8-11
a wiring formed over the second insulating film including nitrogen.	Page 10, line 20

(VI) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1 and 12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Arita et al. (U.S. Patent No. 6,046,490) in view of Zhang (U.S. Patent No. 5,990,491). Claims dependent from claims 1 and 12 are further rejected; however, Appellant appeals the rejection of the parent claims without further argument with respect to the dependent claims.

Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Mochizuki et al. (U.S. Patent No. 5,990,507) in view of Arita et al. and Zhang. Claims dependent from claim 5 are further rejected; however, Appellant appeals the rejection of the parent claims without further argument with respect to the dependent claims.

(VII) ARGUMENTS

Appellant respectfully disagrees with rejections under §103. Appellant notes that none of the cited references, alone or in proper combination, teach or suggest each and every claimed limitation of the claimed invention.

With respect to the rejection of claims 1, 5 and 12, the claimed limitation of "nitrogen all over the planarized surface of the silicon oxide film" is not met by the cited combination of references.

Claims 1 and 12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Arita et al. (U.S. Patent No. 6,046,490) in view of Zhang (U.S. Patent No. 5,990,491).

Appellant respectfully disagrees with this rejection because, even if the cited references were properly combined, the combination would not teach each and every element of the claimed invention.

The invention of claims 1, 5 and 12 includes a planarized SiO layer with a nitrogen layer residing all over the planarized layer, and then a wiring layer formed over the planarized surface including nitrogen.

The Examiner asserts that Arita et al. shows in Fig. 1 a wiring (24a, 24b) directly over a SiO layer (22), and the combination of the wire and layer is subsequently covered with a layer that could be SiN.

However, because the layer of Arita et al. is subsequently added after the wiring layer, it can not be said to be have nitrogen residing all over the planarized surface of the silicon oxide film. The nitrogen would cover the wiring in the area of the wiring, and the area below the

wiring of Arita et al. must necessarily be devoid of the later-added nitrogen. Therefore, this limitation is not taught or suggested by the cited references or combination of references.

Further with respect to the rejection of claim 5, the claimed limitation of the "wiring formed *over the fourth insulation film including nitrogen*" is not met by the cited combination of references

Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Mochizuki et al. (U.S. Patent No. 5,990,507) in view of Arita et al. and Zhang.

The Examiner admits that Arita et al. does not specifically show that a wiring layer is positioned above the silicon nitride film including nitrogen. However, the Examiner notes that Fig. 5 of Zhang shows a contact (510) formed over a nitrogen-containing passivation layer. The Examiner concludes that it would have been obvious to modify the device of Arita by adding an upper contact above the silicon nitride passivation film as taught by Zhang to provide an electrical connection to the lower semiconductor components. Presumably, the Examiner is considering a contact as the same as a wiring layer.

However, Appellant submits that the Examiner's comparison of the cited combination to the present invention is incorrect because the contact (510) of Zhang is not equivalent to the claimed wiring layer. The Examiner notes that Zhang shows a contact that penetrates through the insulating layer to reach a lower P-type drain (507). However, Appellant submits that this is not equivalent to a wiring over the insulating layer, as in the present invention. Therefore, not all of the claimed limitations are taught or disclosed by the cited reference.

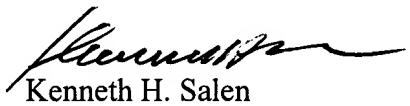
Summary

Appellant respectfully submits that the rejection of the independent claims 1, 5 and 12, and claims dependent therefrom, should be withdrawn because not all of the claimed limitations are taught by the cited references and combination of references. Favorable treatment of this appeal is requested.

If this paper is not timely filed, Appellant hereby petitions for an appropriate extension of time. The fee for any such extension, and any other fees that are required with respect to this paper, may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



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(VIII) CLAIMS APPENDIX

The claims on appeal are numbered 1 through 12, and read as follows:

1. (Previously Presented) A semiconductor device, comprising:

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed over the semiconductor substrate;

a first insulating film formed over the transistor;

a capacitor formed over the first insulating film, the capacitor having a dielectric film made of one of a ferroelectric material and a high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;

silicon oxide film formed over the capacitor to form a planarized surface; wherein nitrogen resides all over the planarized surface of the silicon oxide film; and

a wiring formed over the silicon oxide including nitrogen.

2. (Previously Presented) A semiconductor device according to claim 1, wherein cavities are formed inside of the silicon oxide film.

3. (Previously Presented) A semiconductor device according to claim 1, further comprising,

a second insulating film formed between the capacitor and the silicon oxide film; and a wiring formed on the second insulating film.

4. (Previously Presented) A semiconductor device according to claim 2, further comprising:

a third insulating film formed on the silicon oxide film.

5. (Previously Presented) A semiconductor device, comprising:

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed over the semiconductor substrate;

a first insulating film formed over the transistor;

a capacitor formed over the first insulating film, the capacitor having a dielectric made of one of ferroelectric material and a high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;

a second insulating film formed over the capacitor;

a local interconnection formed over the second insulating film to electrically connect the upper electrode of the capacitor with the first impurity region;

a third insulating film formed over the local interconnection and the second insulating film;

a first wiring formed over the third insulating film and electrically connected to the second impurity region via a hole which is formed over the first insulating film, the second insulating film, and the third insulating film;

a fourth insulating film formed over the first wiring to serve an upper planarized surface, wherein nitrogen resides all over the upper planarized surface of the fourth insulating film; and

a second wiring formed over the fourth insulating film including nitrogen.

6. (Previously Presented) A semiconductor device according to claim 5, wherein cavities, a part of which are exposed from the upper surface of the fourth insulating film, are formed inside of the fourth insulating film.

7. (Original) A semiconductor device according to claim 6, wherein the cavities are located in regions between a plurality of capacitors.

8. (Original) A semiconductor device according to claim 6, further comprising:

a fifth insulating film formed on the fourth insulating film to cover the cavities which are exposed from the upper surface of the fourth insulating film.

9. (Original) A semiconductor device according to claim 5, wherein the second wiring is connected to the first wiring via the hole formed in the fourth insulating film.

10. (Original) A semiconductor device according to claim 5, wherein the third insulating film and the fourth insulating film are formed of a silicon oxide film.

11. (Original) A semiconductor device according to claim 5, wherein an upper surface of the first insulating film is a planarized surface.

12. (Previously Presented) A semiconductor device, comprising:

a transistor having a first impurity region and a second impurity region formed over a semiconductor substrate, and a gate electrode formed over the semiconductor substrate;

a first insulating film formed over the transistor;

a capacitor formed over the first insulating film, the capacitor having a dielectric film made of one of a ferroelectric material and a high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween; and

a second insulating film formed over the capacitor to serve as an upper planarized surface; wherein nitrogen resides all over the upper planarized surface of the second insulating film; and

a wiring formed over the second insulating film including nitrogen.

13. (Withdrawn) A method of manufacturing a semiconductor device comprising the steps of:

forming a transistor on a semiconductor substrate;

forming a first insulating film on the semiconductor substrate to cover the transistor;

forming a capacitor, which includes a dielectric film formed of either a ferroelectric material or a high-dielectric material and an upper electrode and a lower electrode formed to put the dielectric film therebetween, on the first insulating film;

forming a second insulating film over the capacitor;

planarizing an upper surface by polishing the second insulating film; and

applying a dehydration process to the second insulating film by plasma annealing.

14. (Withdrawn) A method according to claim 13, wherein the plasma annealing is performed by plasmanizing a single gas of one of N_2O, N_2, NO, and O_2.

15. (Withdrawn) A method of manufacturing a semiconductor device according to claim 13, wherein the second insulating film is formed by a plasma enhanced CVD method using a TEOS gas.

16. (Withdrawn) A method of manufacturing a semiconductor device according to claim 13, wherein cavity is formed in the second insulating film.

17. (Withdrawn) A method of manufacturing a semiconductor device according to claim 16, wherein upper portions of cavity is exposed by polishing the second insulating film.

18. (Withdrawn) A method of manufacturing a semiconductor device according to claim 13, further comprising the step of:

forming a third insulating film on the second insulating film after the dehydration process.

19. (Withdrawn) A method of manufacturing a semiconductor device according to claim 13, further comprising the step of:

forming a fourth insulating film between the capacitor and the second insulating film to cover the capacitor; and

forming a wiring between the second insulating film and the fourth insulating film.

(IX) EVIDENCE APPENDIX

Not applicable.

(X) RELATED PROCEEDINGS APPENDIX

Not applicable.